

REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow.

Since this response has been filed within two months after the August 14, 2006, mailing date of the Final Rejection in this application, a timely Advisory Action is requested.

In the August 14, 2006, Final Rejection, the Examiner rejected claims 9-11 and 13-16 under 35 U.S.C. §103(a) as being unpatentable over the Yama '657 reference in view of Applicant's Prior Art in the specification. Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over the Yama reference and Applicants' Prior Art and further in view of the Wolf reference.

As indicated above, claims 9-16 have been cancelled. Claims 17-26 have been added. For the reasons set forth below, Applicant submits that new claims 17-26 patentably distinguish over the reference combinations cited by the Examiner.

As previously stated, the present invention is directed to an ultra low leakage MOSFET transistor that is formed to minimize band-to-band and trap-assisted tunneling mechanisms that exist in prior art devices and can lead to gate induced drain leakage in the MOSFET transistor. In accordance with the invention, this design improvement is obtained by providing a new conductive gate electrode structure. As show in Fig. 3 of the application, the conductive gate electrode of the claimed MOSFET transistor includes a first portion that extends over the substrate channel region and a second portion that extends continuously over the entire substantially rectangular interface between the isolation dielectric material and the active device region that the isolation dielectric material defines.

The Examiner again relies on the Yama '657 patent to provide this teaching. In response, Applicant has cancelled claims 9-16 and provided new claims 17-23 that are directed to a structure "consisting of" the structure shown in Applicant's Fig. 3 and new claims 24-26 that are directed to a method that results in a structure "consisting of" the Fig. 3 structure. That is, the MOSFET recited in new claims 17-26 includes a single source region and a single drain region formed in a single active device region.

As previously discussed, the Yama reference discloses a MOSFET transistor structure in which the "drain" includes a multiplicity of drain diffusion regions formed in the substrate and the "source" also includes a multiplicity of source diffusion regions formed in the same active device substrate. The gate electrode is a one solid piece of conductive material that extends over the entire active device region, except for open portions that expose the multiple drain regions and the multiple source regions so that a conductive interconnect structure be dropped down through vias in the dielectric material to contact the multiple drain regions and the multiple source regions. This is completely unlike Applicant's claimed Fig. 3 structure.

In view of the above, Applicant submits that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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